

FDP8870_F085

N-Channel PowerTrench® MOSFET 30V, 156A, 4.1mΩ

General Description

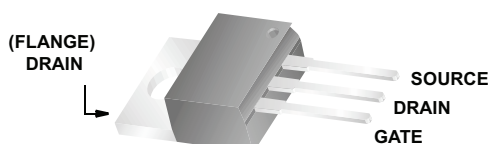
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.

Features

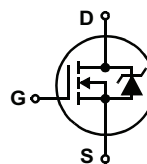
- $r_{DS(ON)} = 4.1m\Omega$ $V_{GS} = 10V$, $I_D = 35A$
- $r_{DS(ON)} = 4.6m\Omega$ $V_{GS} = 4.5V$, $I_D = 35A$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- Qualified to AEC Q101
- RoHS Compliant

Applications

- DC/DC converters



TO-220AB
FDP SERIES



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Note 1)	156	A
	Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 4.5V$) (Note 1)	147	A
	Continuous ($T_{amb} = 25^\circ\text{C}$, $V_{GS} = 10V$, with $R_{\theta JA} = 62^\circ\text{C/W}$)	19	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	300	mJ
P_D	Power dissipation	160	W
	Derate above 25°C	1.07	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-220	0.94	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220 (Note 3)	62	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8870	FDP8870_F085	TO-220AB	Tube	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35\text{A}$, $V_{GS} = 10\text{V}$	-	0.0034	0.0041	Ω
		$I_D = 35\text{A}$, $V_{GS} = 4.5\text{V}$	-	0.0040	0.0046	
		$I_D = 35\text{A}$, $V_{GS} = 10\text{V}$, $T_J = 175^\circ\text{C}$	-	0.0051	0.0065	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	5200	-	pF
C_{OSS}	Output Capacitance		-	970	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	570	-	pF
R_G	Gate Resistance	$V_{GS} = 0.5\text{V}$, $f = 1\text{MHz}$	-	2.1	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	-	106	132	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V	-	56	69	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V	-	5.0	6.5	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	-	15	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	10	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	23	-	nC
			-		-	

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}$, $I_D = 35\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 3.3\Omega$	-	-	168	ns
$t_{d(ON)}$	Turn-On Delay Time		-	11	-	ns
t_r	Rise Time		-	105	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	70	-	ns
t_f	Fall Time		-	46	-	ns
t_{OFF}	Turn-Off Time		-	-	173	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 35\text{A}$	-	-	1.25	V
		$I_{SD} = 15\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	37	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 35\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	21	nC

Notes:

- 1: Package current limitation is 80A.
- 2: Starting $T_J = 25^\circ\text{C}$, $L = 0.15\text{mH}$, $I_{AS} = 64\text{A}$, $V_{DD} = 27\text{V}$, $V_{GS} = 10\text{V}$.
- 3: Pulse width = 100s.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

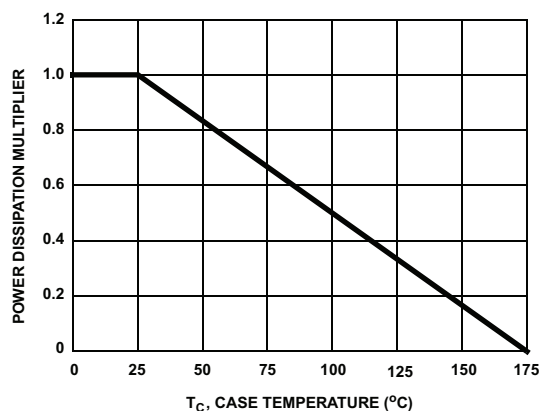


Figure 1. Normalized Power Dissipation vs Case Temperature

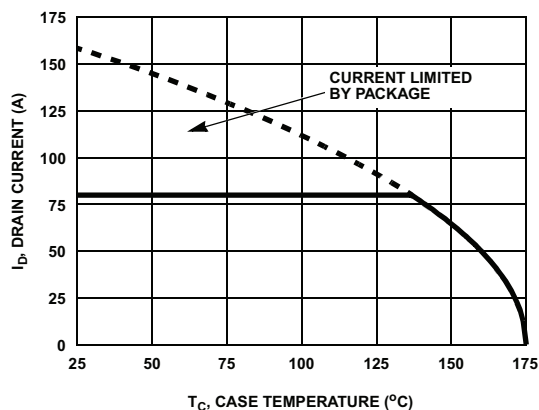


Figure 2. Maximum Continuous Drain Current vs Case Temperature

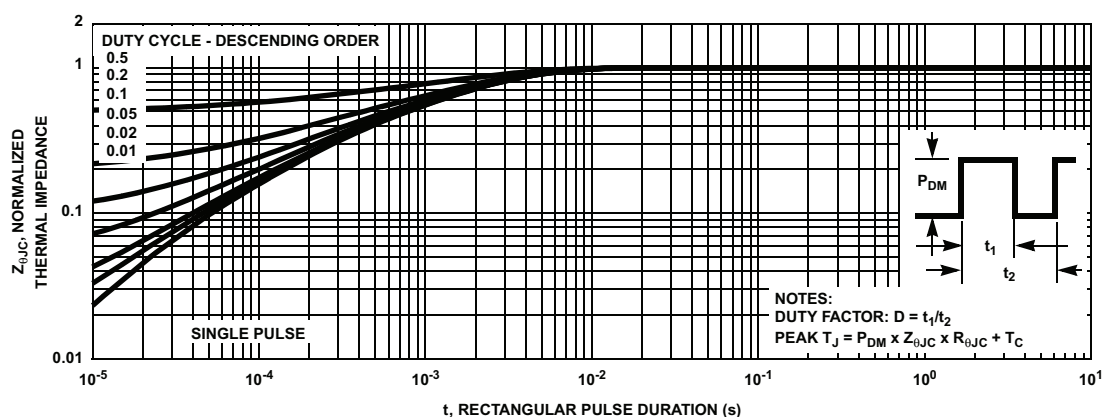


Figure 3. Normalized Maximum Transient Thermal Impedance

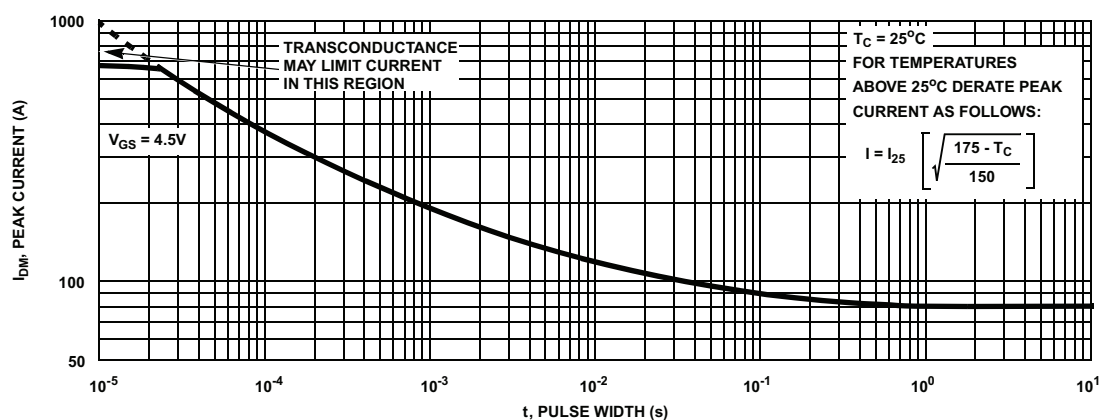


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

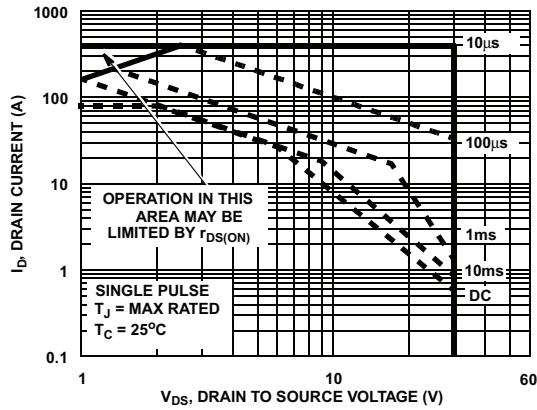
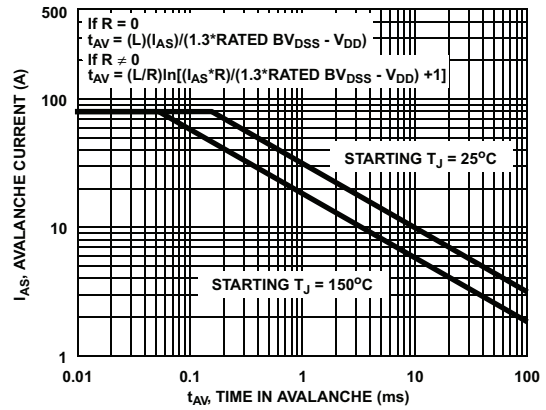


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

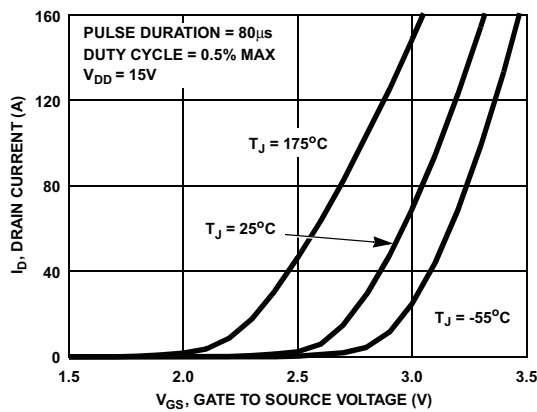


Figure 7. Transfer Characteristics

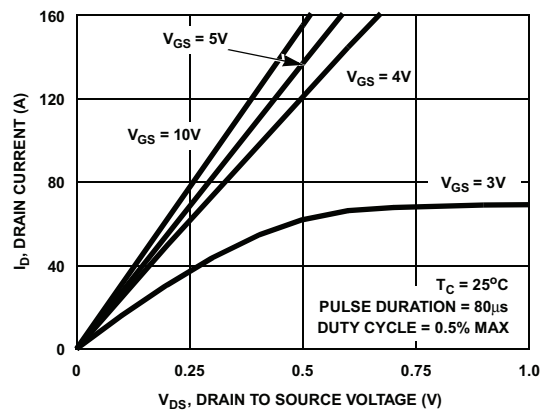


Figure 8. Saturation Characteristics

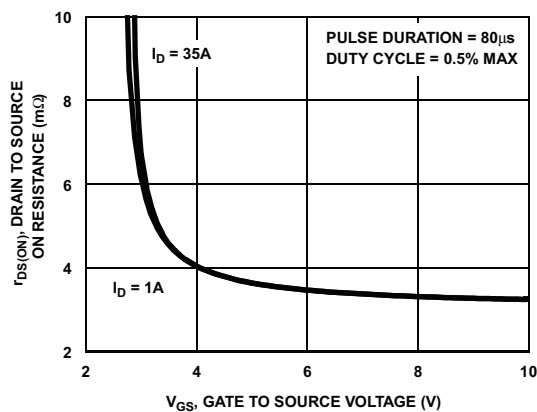


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

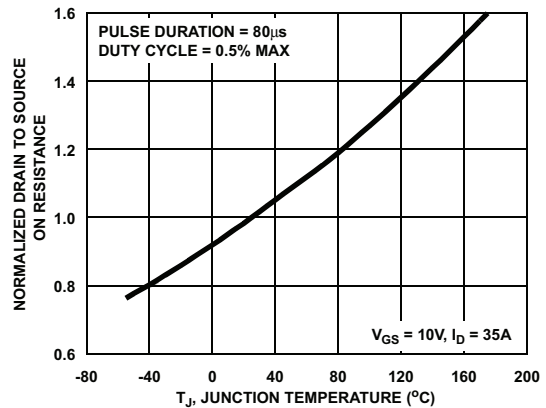


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

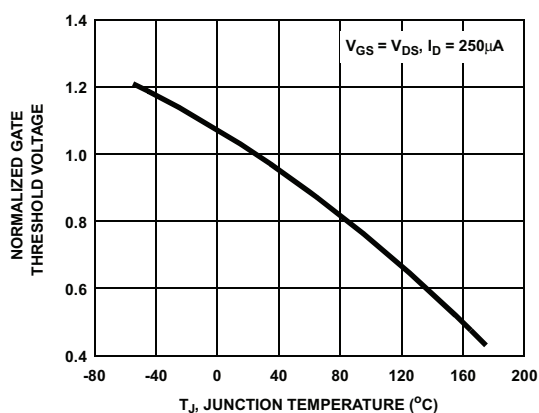


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

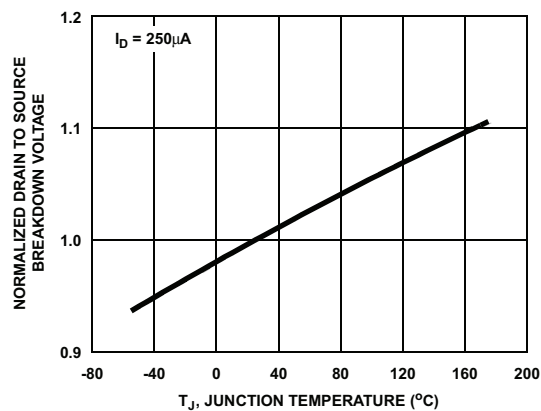


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

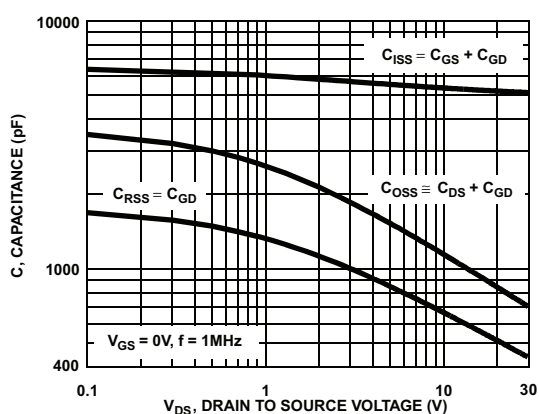


Figure 13. Capacitance vs Drain to Source Voltage

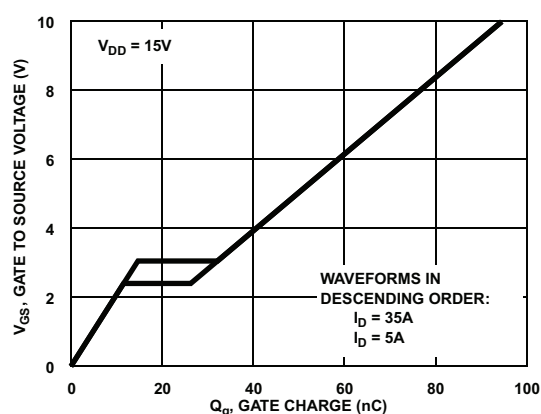


Figure 14. Gate Charge Waveforms for Constant Gate Current

Test Circuits and Waveforms

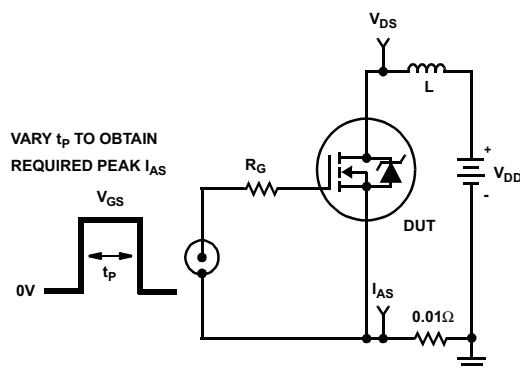


Figure 15. Unclamped Energy Test Circuit

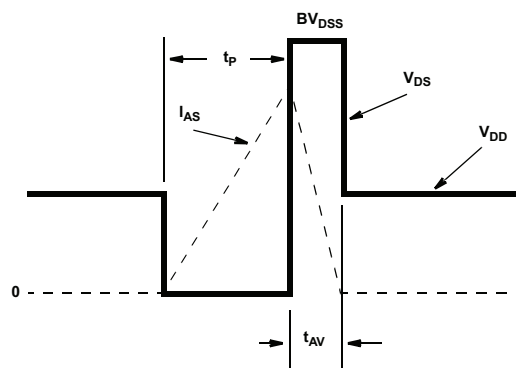


Figure 16. Unclamped Energy Waveforms

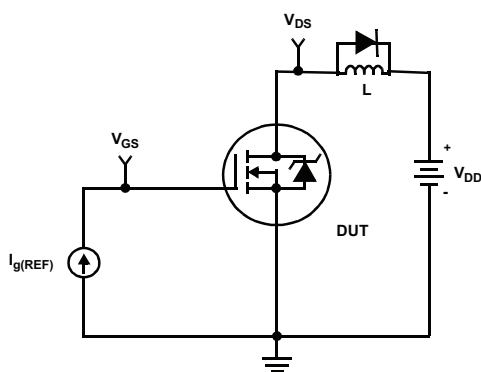


Figure 17. Gate Charge Test Circuit

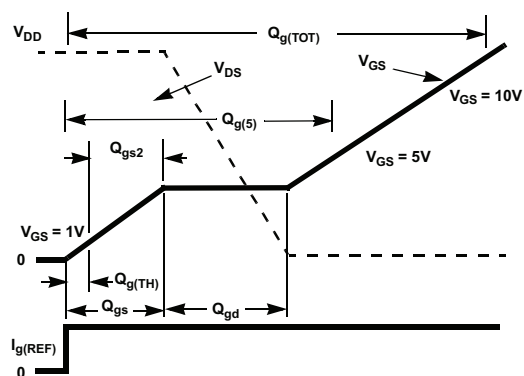


Figure 18. Gate Charge Waveforms

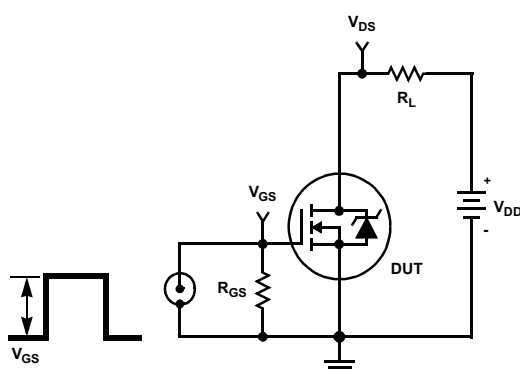


Figure 19. Switching Time Test Circuit

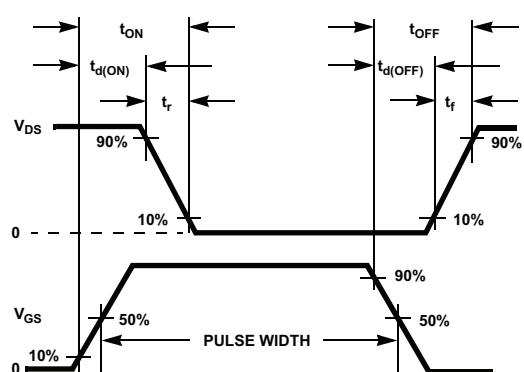


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDP8870 2 1 3 ; rev December 2003

Ca 12 8 4.5e-9

Cb 15 14 4.5e-9

Cin 6 8 4.7e-9

Dbody 7 5 DbodyMOD

Dbreak 5 11 DbreakMOD

Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 33.45

Eds 14 8 5 8 1

Egs 13 8 6 8 1

Esg 6 10 6 8 1

Evthres 6 21 19 8 1

Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 3.6e-9

Ldrain 2 5 1.0e-9

Lsource 3 7 3.3e-9

RLgate 1 9 36

RLdrain 2 5 10

RLsource 3 7 33

Mmed 16 6 8 8 MmedMOD

Mstro 16 6 8 8 MstroMOD

Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1

Rdrain 50 16 RdrainMOD 2.15e-3

Rgate 9 20 2.1

RSLC1 5 51 RSLCMOD 1e-6

RSLC2 5 50 1e3

Rsource 8 7 RsourceMOD 9e-4

Rvthres 22 8 RvthresMOD 1

Rvtemp 18 19 RvtempMOD 1

S1a 6 12 13 8 S1AMOD

S1b 13 12 13 8 S1BMOD

S2a 6 15 14 13 S2AMOD

S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE=({(V(5,51)/ABS(V(5,51)))}*(PWR(V(5,51)/(1e-6*500),10)))

.MODEL DbodyMOD D (IS=7.5E-12 IKF=17 N=1.01 RS=2.1e-3 TRS1=2e-3 TRS2=2e-7

+ CJO=1.9e-9 M=0.57 TT=9e-11 XTI=2.6)

.MODEL DbreakMOD D (RS=8e-2 TRS1=1e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=1.75e-9 IS=1e-30 N=10 M=0.4)

.MODEL MmedMOD NMOS (VTO=2.1 KP=30 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.1 T_ABS=25)

.MODEL MstroMOD NMOS (VTO=2.51 KP=650 IS=1e-30 N=10 TOX=1 L=1u W=1u T_ABS=25)

.MODEL MweakMOD NMOS (VTO=1.67 KP=0.1 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=21 RS=0.1 T_ABS=25)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-9e-7)

.MODEL RdrainMOD RES (TC1=2.3e-3 TC2=5e-6)

.MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)

.MODEL RsourceMOD RES (TC1=8e-3 TC2=1e-6)

.MODEL RvthresMOD RES (TC1=-2.3e-3 TC2=-9e-6)

.MODEL RvtempMOD RES (TC1=-3e-3 TC2=2e-7)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-2)

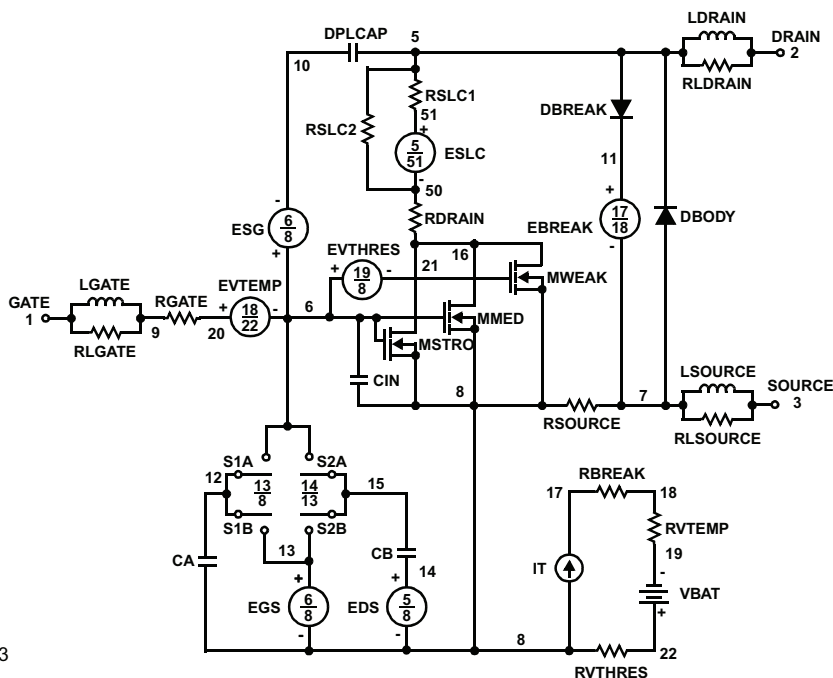
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1 VOFF=-0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=-1)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

rev December 2003

template FDP8870 n2,n1,n3 = m_temp

electrical n2,n1,n3

number m_temp=25

{

var i iscl

dp..model dbodymod = (isl=7.5e-12,ikf=17,nl=1.01,rs=2.1e-3,trs1=2e-3,trs2=2e-7,cjo=1.9e-9,m=0.57,tt=9e-11,xti=2.6)

dp..model dbreakmod = (rs=8e-2,trs1=1e-3,trs2=-8.9e-6)

dp..model dplcapmod = (cjo=1.75e-9,isl=10e-30,nl=10,m=0.4)

m..model mmedmod = (type=_n,vto=2.1,kp=30,rs=1e-30, tox=1)

m..model mstrongmod = (type=_n,vto=2.51,kp=650,rs=1e-30, tox=1)

m..model mweakmod = (type=_n,vto=1.67,kp=0.1,rs=1e-30, tox=1,rs=0.1)

sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-2)

sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-2,voff=-4)

sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1,voff=-0.5)

sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-1)

c.ca n12 n8 = 4.5e-9

c.cb n15 n14 = 4.5e-9

c.cin n6 n8 = 4.7e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 33.45

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 3.6e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 3.3e-9

res.rlgate n1 n9 = 36

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 33

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u, temp=m_temp

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u, temp=m_temp

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u, temp=m_temp

res.rbreak n17 n18 = 1, tc1=8.3e-4,tc2=-9e-7

res.rdrain n50 n16 = 2.15e-3, tc1=2.3e-3,tc2=5e-6

res.rgate n9 n20 = 2.1

res.rslc1 n5 n51 = 1e-6, tc1=1e-4,tc2=1e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 9e-4, tc1=8e-3,tc2=1e-6

res.rvthres n22 n8 = 1, tc1=-2.3e-3,tc2=-9e-6

res.rvtemp n18 n19 = 1, tc1=-3e-3,tc2=2e-7

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

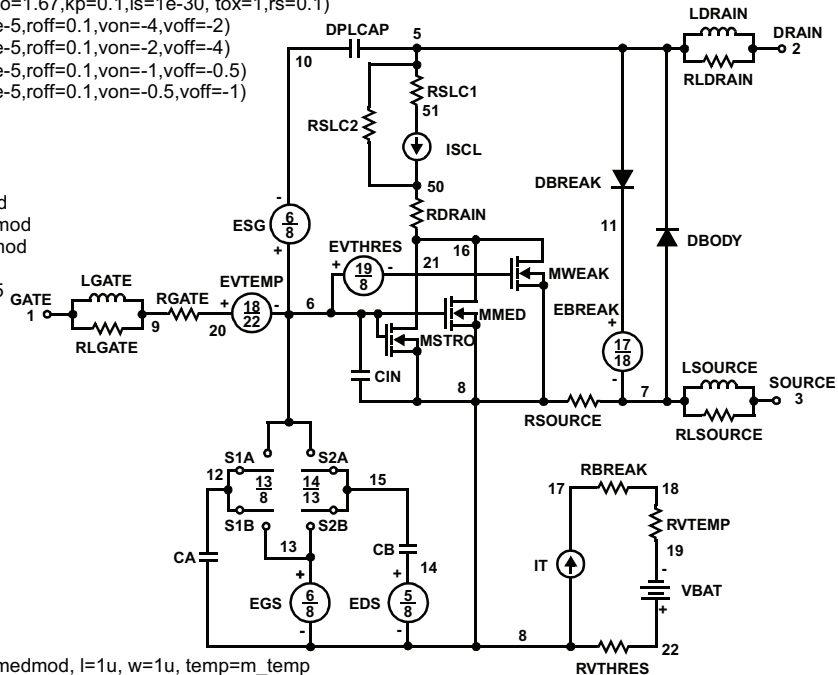
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/500))** 10))

}

}



PSPICE Thermal Model

REV 23 December 2003

FDP8870T

```
CTHERM1 TH 6 1e-3
CTHERM2 6 5 2e-3
CTHERM3 5 4 3e-3
CTHERM4 4 3 9e-3
CTHERM5 3 2 1e-2
CTHERM6 2 TL 2e-2
```

```
RTHERM1 TH 6 3e-2
RTHERM2 6 5 8e-2
RTHERM3 5 4 1.1e-1
RTHERM4 4 3 1.6e-1
RTHERM5 3 2 1.72e-1
RTHERM6 2 TL 2e-1
```

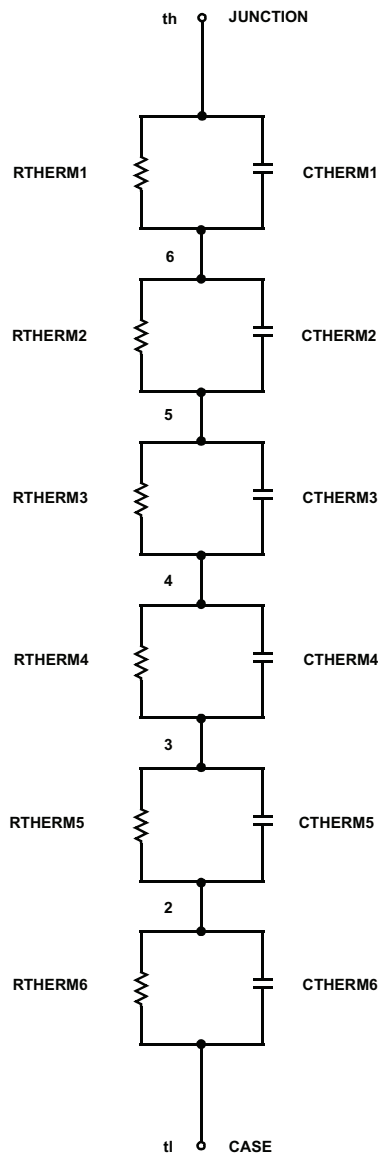
SABER Thermal Model

SABER thermal model FDP8870T

template thermal_model th tl
thermal_c th, tl

```
{
  ctherm.ctherm1 th 6 =1e-3
  ctherm.ctherm2 6 5 =2e-3
  ctherm.ctherm3 5 4 =3e-3
  ctherm.ctherm4 4 3 =9e-3
  ctherm.ctherm5 3 2 =1e-2
  ctherm.ctherm6 2 tl =2e-2
```

```
rtherm.rtherm1 th 6 =3e-2
rtherm.rtherm2 6 5 =8e-2
rtherm.rtherm3 5 4 =1.1e-1
rtherm.rtherm4 4 3 =1.6e-1
rtherm.rtherm5 3 2 =1.72e-1
rtherm.rtherm6 2 tl =2e-1
}
```





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CorePLUS™	Green FPS™	Programmable Active Droop™	TinyBoost™
CorePOWER™	Green FPS™ e-Series™	QFET®	TinyBuck™
CROSSVOLT™	Gmax™	QS™	TinyCalc™
CTL™	GTO™	Quiet Series™	TinyLogic®
Current Transfer Logic™	IntelliMAX™	RapidConfigure™	TINYOPTO™
DEUXPEED®	ISOPLANAR™	 Saving our world, 1mW/W/kW at a time™	TinyPower™
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EcoSPARK®	MICROCOUPLER™	SmartMax™	TinyWire™
EfficientMax™	MicroFET™	SMART START™	TriFault Detect™
ESBC™	MicroPak™	SPM®	TRUECURRENT™*
 Fairchild®	MicroPak2™	STEALTH™	µSerDes™
Fairchild Semiconductor®	MillerDrive™	SuperFET™	 SerDes®
FACT Quiet Series™	MotionMax™	SuperSOT™-3	UHC®
FACT®	Motion-SPM™	SuperSOT™-6	Ultra FRFET™
FAST®	OptoHit™	SuperSOT™-8	UniFET™
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FPS™			

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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