

# FDP045N10A\_F102 / FDI045N10A\_F102

## N-Channel PowerTrench® MOSFET

100V, 164A, 4.5mΩ

### Features

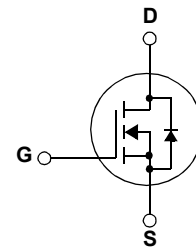
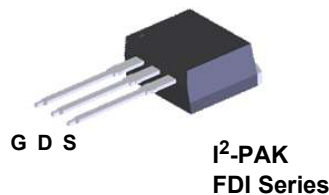
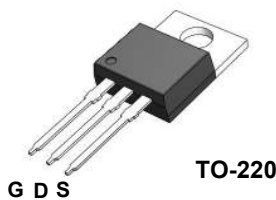
- $R_{DS(on)} = 3.8m\Omega$  (Typ.) @  $V_{GS} = 10V$ ,  $I_D = 100A$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Application

- DC to DC Converters
- Synchronous Rectification for Telecommunication PSU
- Battery Charger
- AC motor drives and Uninterruptible Power Supplies
- Off-line UPS



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDP045N10A_F102 FDI045N10A_F102	Units
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	A
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	
		- Continuous ( $T_C = 25^\circ\text{C}$ , Package Limited)	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	W
		- Derate above $25^\circ\text{C}$	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

### Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.57	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP045N10A	FDP045N10A_F102	TO-220	-	-	50
FDI045N10A	FDI045N10A_F102	I2PAK	-	-	50

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	100	-	-	V
$\Delta BV_{DSS}$ $\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.07	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = 80\text{V}$ , $T_C = 150^\circ\text{C}$	-	-	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 100\text{A}$	-	3.8	4.5	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}$ , $I_D = 100\text{A}$ (Note 4)	-	132	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	3960	5270	pF
$C_{oss}$	Output Capacitance		-	925	1230	pF
$C_{rss}$	Reverse Transfer Capacitance		-	34	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$	-	1520	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{GS} = 10\text{V}$ , $V_{DS} = 50\text{V}$ $I_D = 100\text{A}$ (Note 4, 5)	-	57	74	nC
$Q_{gs}$	Gate to Source Gate Charge		-	17	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	8	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	13	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{V}$ , $I_D = 100\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GEN} = 4.7\Omega$ (Note 4, 5)	-	23	56	ns
$t_r$	Turn-On Rise Time		-	26	62	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
$t_f$	Turn-Off Fall Time		-	15	40	ns
ESR	Equivalent Series Resistance (G-S)	Drain Open, $f = 1\text{MHz}$	-	1.9	-	$\Omega$

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	164*	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	656	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 100A	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, V <sub>DD</sub> = 50V, I <sub>SD</sub> = 100A	-	75	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs (Note 4)	-	120	-	nC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 3\text{mH}$ ,  $I_{AS} = 20.6\text{A}$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Dual Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

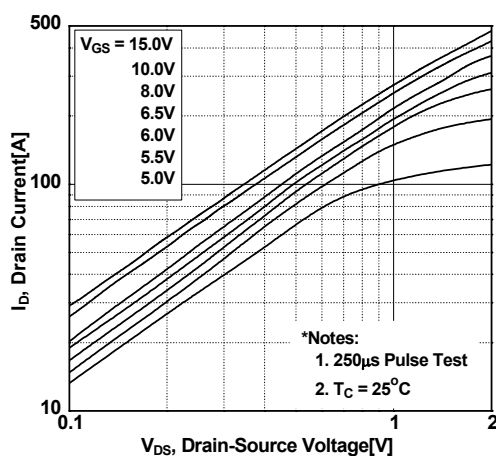


Figure 2. Transfer Characteristics

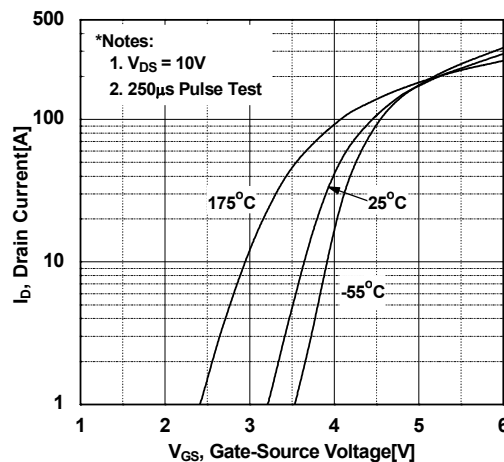


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

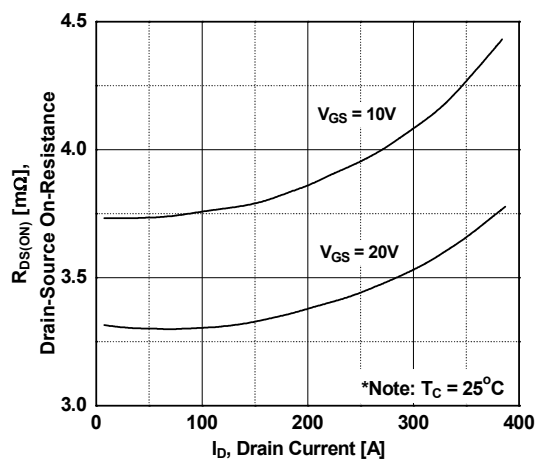


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

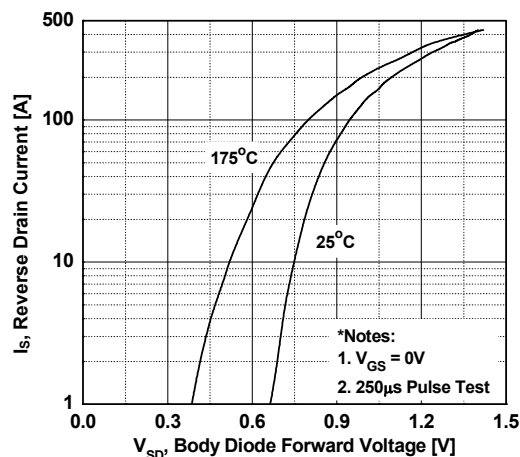


Figure 5. Capacitance Characteristics

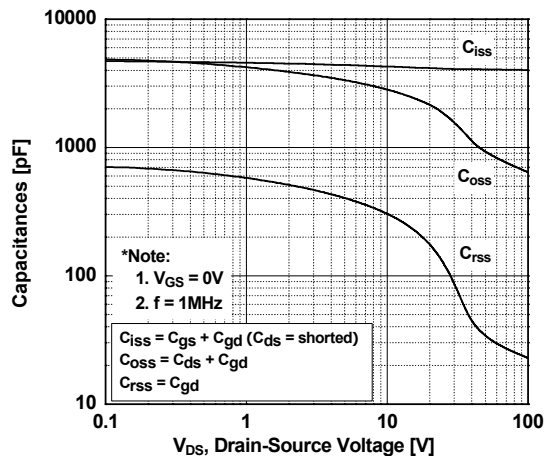
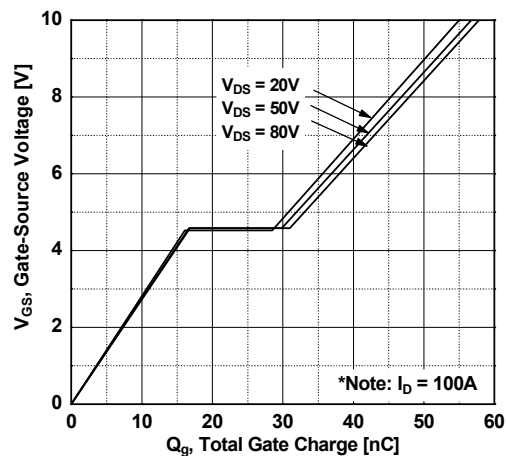


Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

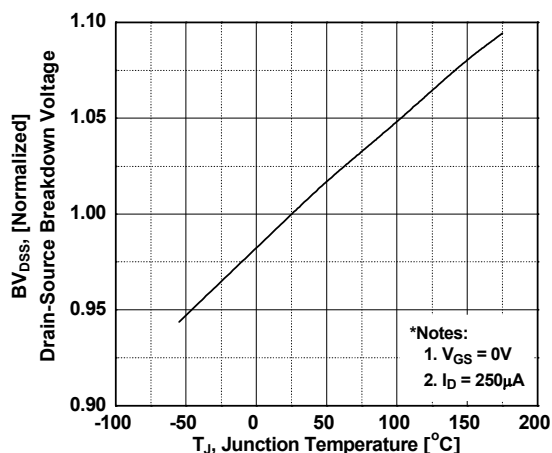


Figure 8. On-Resistance Variation vs. Temperature

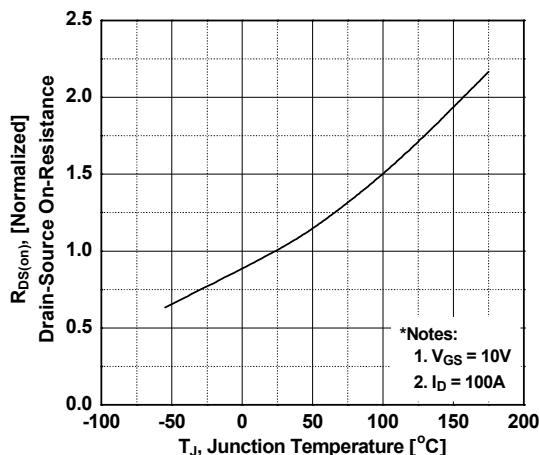


Figure 9. Maximum Safe Operating Area vs. Case Temperature

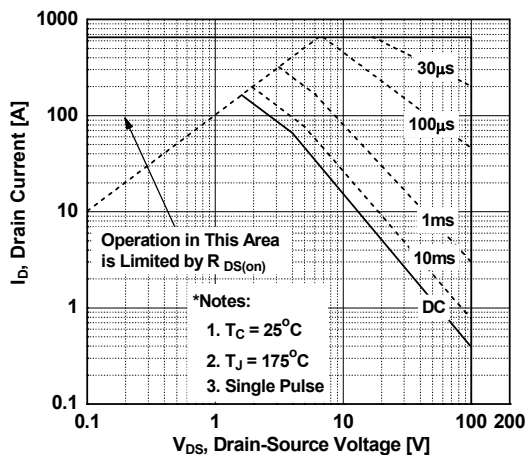


Figure 10. Maximum Drain Current

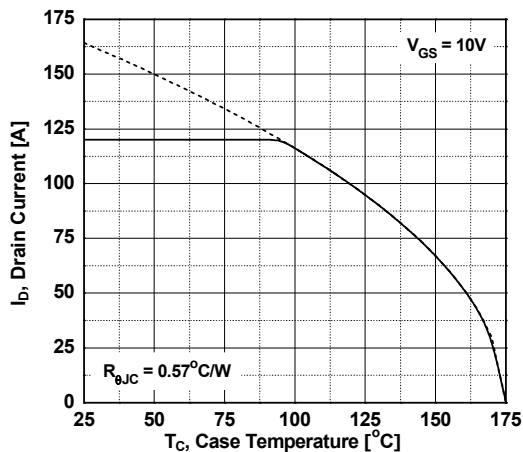


Figure 11. E\_oss vs. Drain to Source Voltage

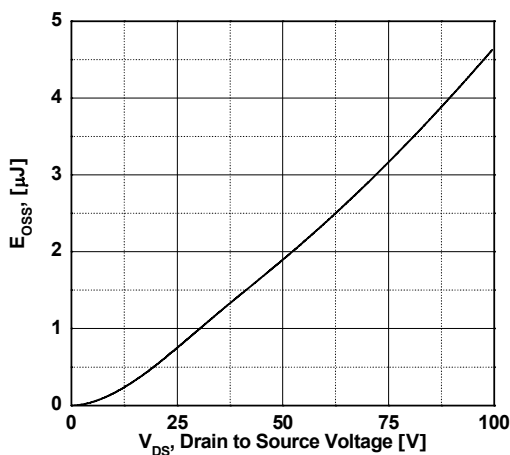
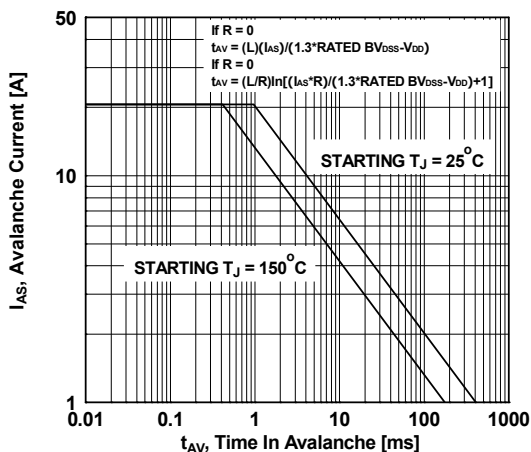
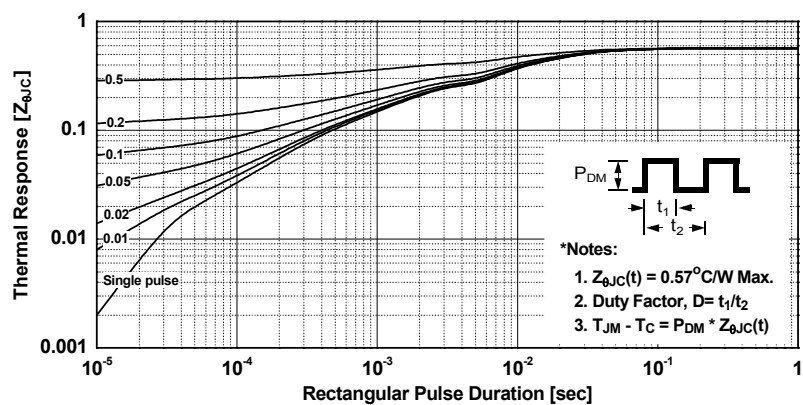


Figure 12. Unclamped Inductive Switching Capability

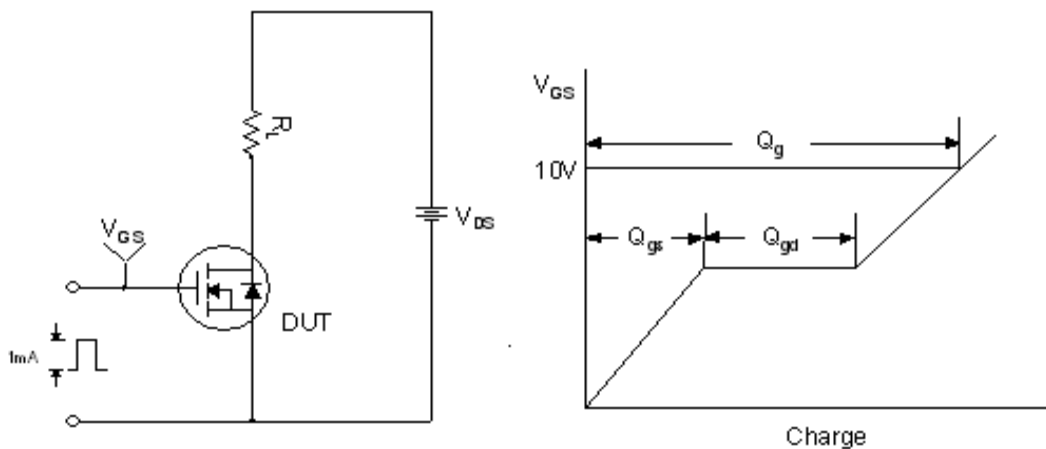


## Typical Performance Characteristics (Continued)

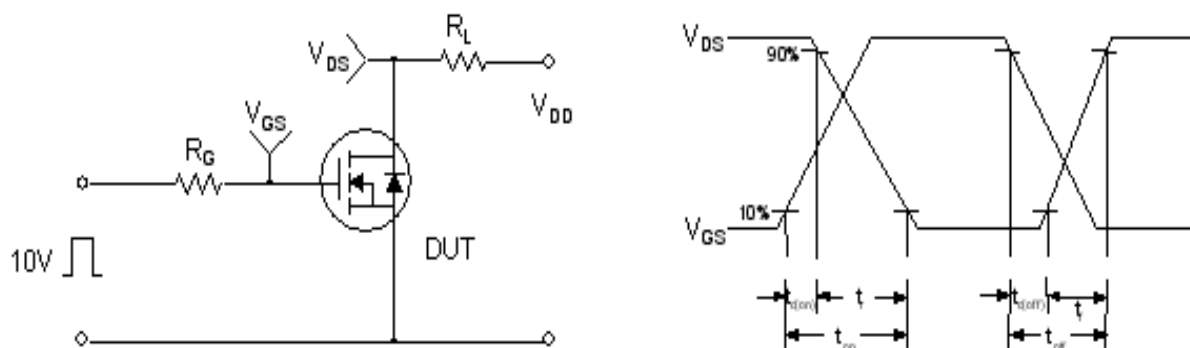
Figure 13. Transient Thermal Response Curve



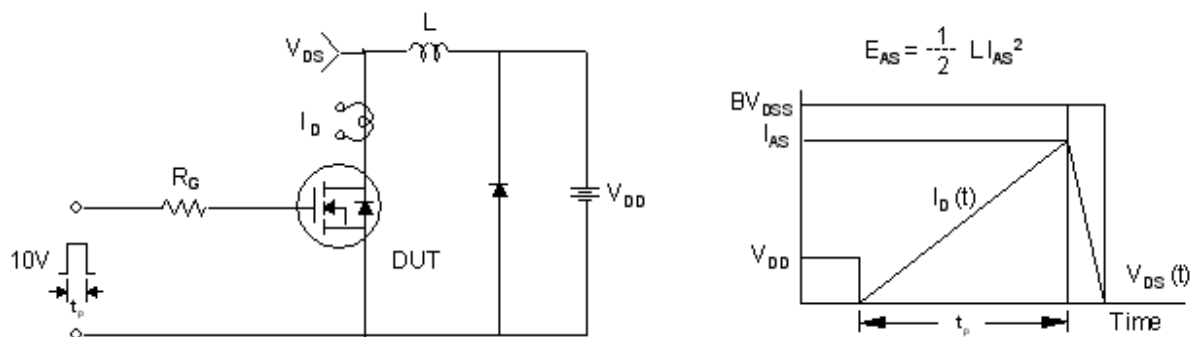
Gate Charge Test Circuit & Waveform



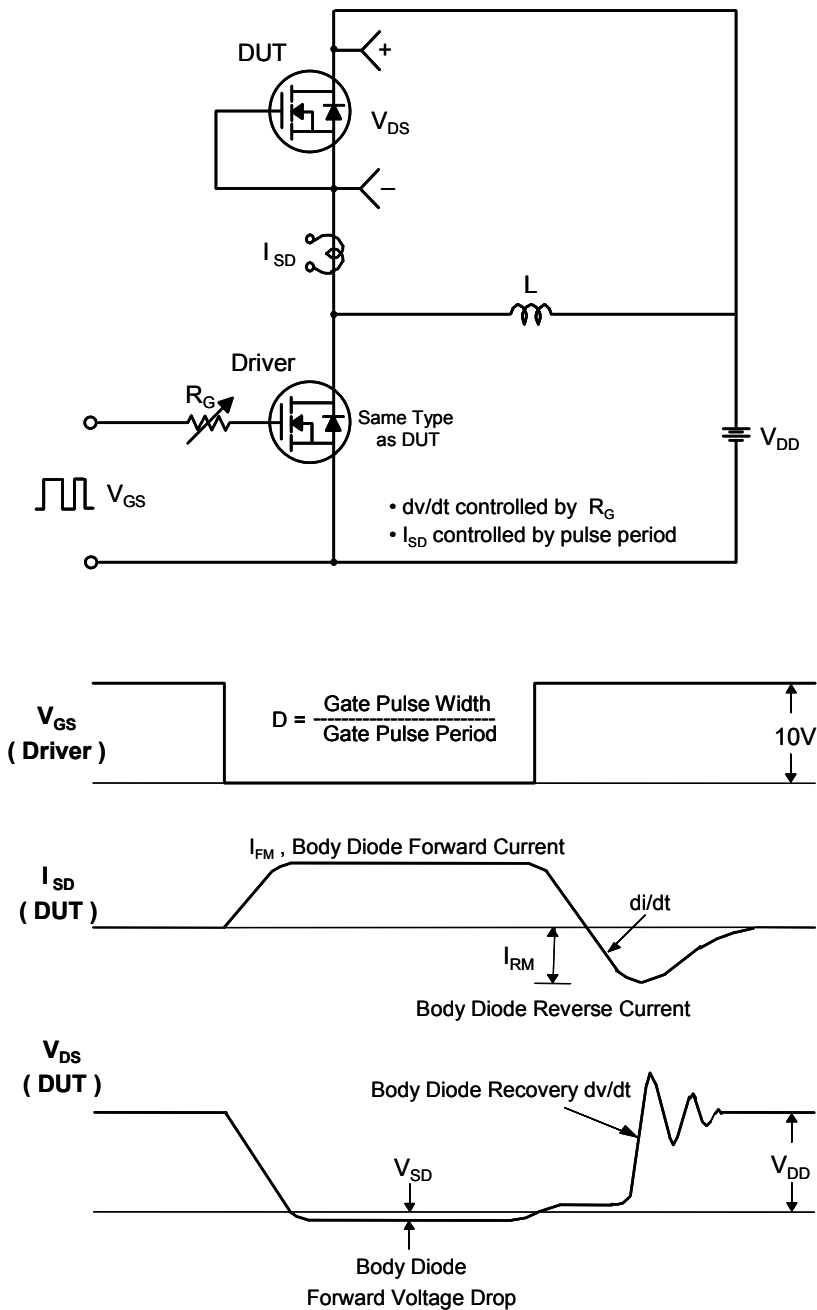
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

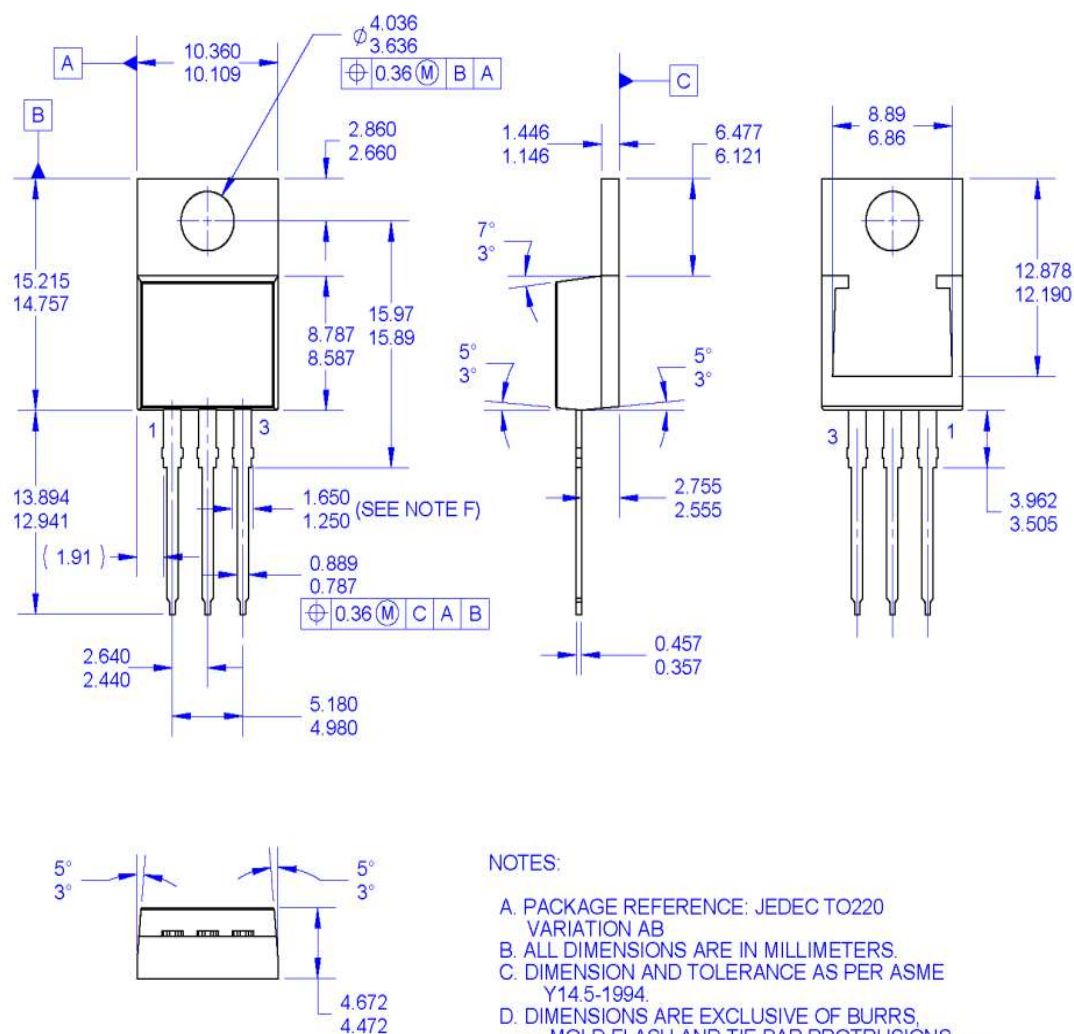


# Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Package Dimensions

# TO-220

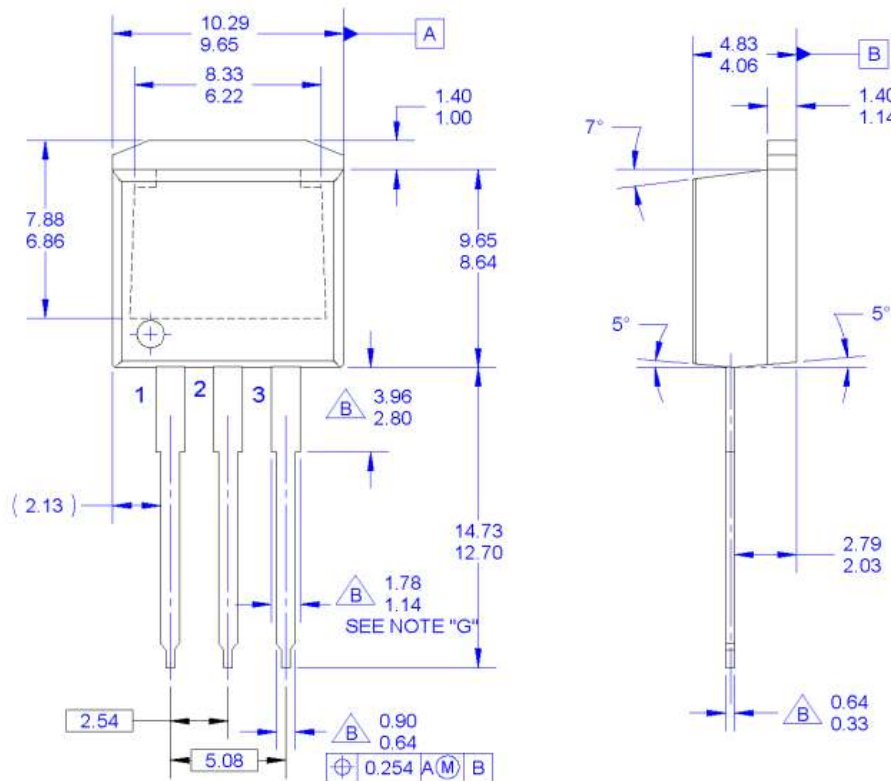


Dimensions in Millimeters



# Package Dimensions

## I2PAK





### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE).
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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